Chapter 9: FET Amplifiers And Switching Circuits

9-1: The Common Source Amplifier (CS Amplifier)

FET has an important advantage compared to the BJT due to the FET's extremely high input impedance. Disadvantages, however, include higher distortion and lower gain. The common-source (CS) amplifier iscomparable to the common-emitter BJT amplifier that you studied in Chapter 6.

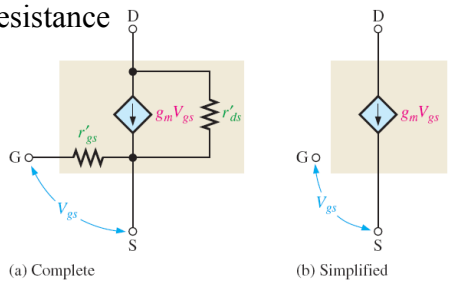
FET AC Model: the ac model for FET is shown below

r_{gs}' is the gate source internal resistance

$g_m V_{gs}$ is the current appear between drain and source

r_{ds}' is the internal drain - to - source resistance

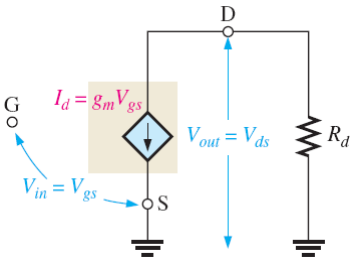
Since r_{gs}' is very large and r_{ds}' is also large → they can be neglected → Simplified model



9-1: The Common Source Amplifier

FET AC Model

An ideal ac circuit model with ac drain resistance R_d can be represented as shown.



The voltage gain for the circuit shown is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{ds}}{V_{gs}}$$

but $V_{ds} = I_d R_d$

and $V_{gs} = \frac{I_d}{g_m}$ ← From definition of transconductance $g_m = I_d/V_{gs}$

$$\rightarrow A_v = \frac{I_d R_d}{I_d/g_m} = \frac{g_m I_d R_d}{I_d}$$

$$\Rightarrow \boxed{A_v = g_m R_d}$$

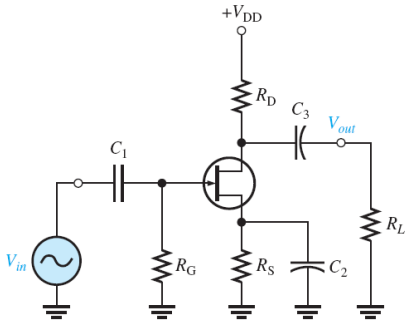
Ex: for a JFET with $g_m = 4\text{mS}$ and $R_d = 1.5\text{k}\Omega$

→ideal voltage gain is $A_v = g_m R_d = (4\text{mS})(1.5\text{k}\ \Omega) = 6$

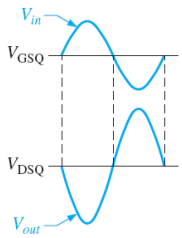
9-1: The Common Source Amplifier

JFET Amplifier Operation

In common source self biased amplifier, V_{in} is applied to the gate and V_{out} is taken from the drain as shown with phase difference between them 180°



(a) Schematic



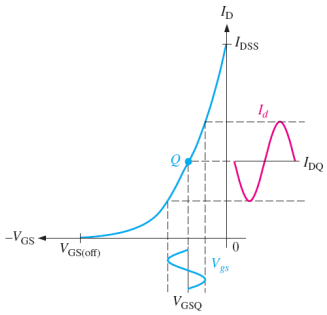
(b) Voltage waveform relationship

Remember that, for ac signal, capacitors are short and V_{DD} is ac ground → source terminal S and R_D are connected to the round in ac equivalent circuit

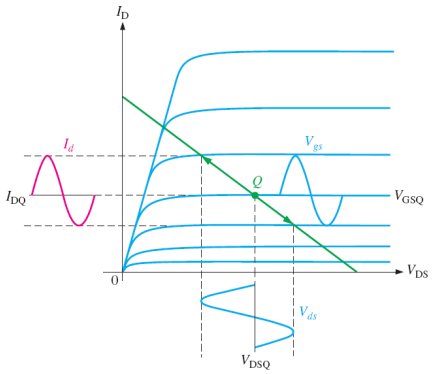
9-1: The Common Source Amplifier

JFET Amplifier Operation: *A Graphical Picture*

the operation of n-channel JFET shown above with V_{in} and V_{out} on I_D characteristic curve and on transfer characteristic curve is shown below



(a) JFET (*n*-channel) transfer characteristic curve showing signal operation



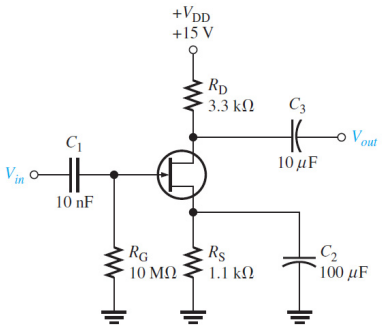
(b) JFET (*n*-channel) drain curves showing signal operation

As V_{gs} varies → Id varies; As V_{gs} decrease (more negative) from Q-point → I_d decreases and As V_{gs} increase → I_d increases. The corresponding change in V_{ds} show the inverse (because $V_D = V_{DD}$-$I_D R_D$).

9-1: The Common Source Amplifier

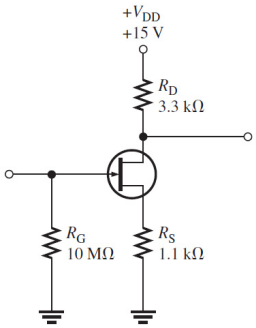
JFET Amplifier Operation: DC Analysis

From the DC equivalent circuit of the amplifier, the Q-point can be found graphically as described before in chapter 8 for the self biased transistor → Once finding I_D you can find V_D



▲ FIGURE 9–5

JFET common-source amplifier.



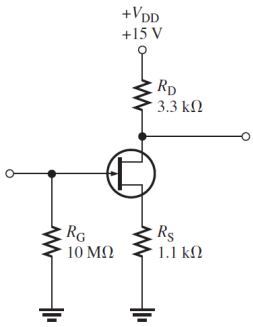
▲ FIGURE 9–6

DC equivalent for the amplifier in Figure 9–5.

9-1: The Common Source Amplifier

JFET Amplifier Operation: DC Analysis: Example

Determine I_D and V_{GS} at the Q-point for the JFET amplifier in Figure 9–6. The typical I_{DSS} for this particular JFET is 4.3 mA and $V_{GS(off)}$ is −7.7 V.

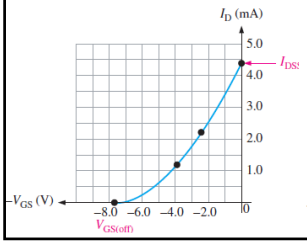


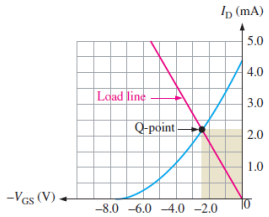
Plot the transconductance curve

$$V_{GS} = 0.3V_{GS(off)} = -2.31\text{ V} \quad \text{when } I_D = \frac{I_{DSS}}{2} = 2.15\text{ mA}$$

$$V_{GS} = 0.5V_{GS(off)} = -3.85\text{ V} \quad \text{when } I_D = \frac{I_{DSS}}{4} = 1.075\text{ mA}$$

Draw the load line from the two points first point (I_D=0 and V_{GS} = 0) and the second point $I_D = I_{DSS}$ and V_{GS} = -$I_D R_S$



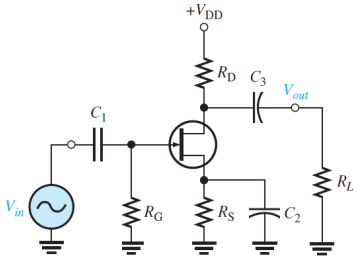


➔ From graph at Q-point, I_D = 2.2 mA and V_{GS} = -2.4 V

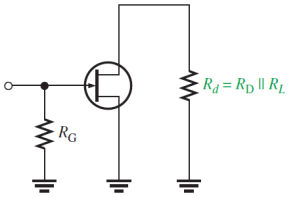
9-1: The Common Source Amplifier

JFET Amplifier Operation: AC Analysis

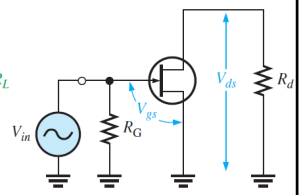
The ac equivalent circuit can be drawn



The amplifier circuit



Ac equivalent circuit



Ac equivalent circuit showing V_{in} and V_{out}

Input resistance

$$R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}}\right) \approx R_G$$

Very small

Output resistance

$R_{out} = R_d$

with no R_L → $R_d = R_D$

With load R_L → $R_d = R_D // R_L$

Voltage gain

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{ds}}{V_{gs}} = g_m R_d$$

9-1: The Common Source Amplifier

JFET Amplifier Operation: AC Analysis - Example

What is the total output voltage for the unloaded amplifier in Figure 9–9? I_{DSS} is 4.3 mA; $V_{GS(off)}$ is −2.7 V; I_{DQ} = 1.91 mA. If a 4.7 kΩ load resistor is ac coupled to the output of the amplifier what is the resulting output voltage?

$$V_D = V_{DD} - I_D R_D = 12\text{ V} - (1.91\text{ mA})(3.3\text{ k}\Omega) = 5.70\text{ V}$$

Next calculate g_m

$$V_{GS} = -I_D R_S = -(1.91\text{ mA})(470\ \Omega) = -0.90\text{ V}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|} = \frac{2(4.3\text{ mA})}{2.7\text{ V}} = 3.18\text{ mS}$$

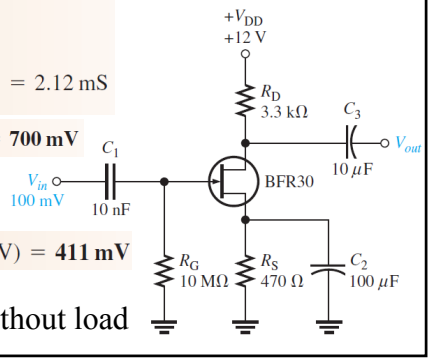
$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = 3.18\text{ mS}\left(1 - \frac{-0.90\text{ V}}{-2.7\text{ V}}\right) = 2.12\text{ mS}$$

$$V_{out} = A_v V_{in} = g_m R_D V_{in} = (2.12\text{ mS})(3.3\text{ k}\Omega)(100\text{ mV}) = \mathbf{700\text{ mV}}$$

If a 4.7 kΩ load resistor is ac coupled to the output of

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (2.12\text{ mS})(1.94\text{ k}\Omega)(100\text{ mV}) = \mathbf{411\text{ mV}}$$

Voltage gain with load < voltage gain without load



9-1: The Common Source Amplifier

JFET Amplifier Operation: AC Analysis - Example

What input resistance is seen by the signal source in Figure 9–11? I_{GSS} = 30 nA at V_{GS} = 10 V.

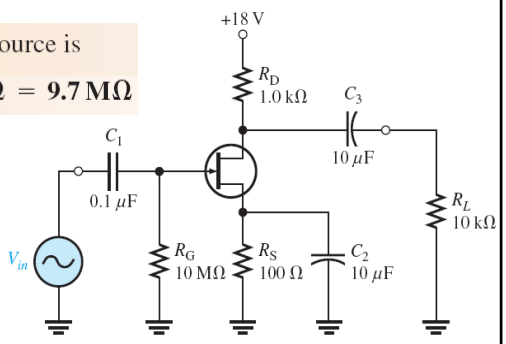
The input resistance at the gate of the JFET is

$$R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{10\text{ V}}{30\text{ nA}} = 333\text{ M}\Omega$$

The input resistance seen by the signal source is

$$R_{in} = R_G \parallel R_{IN(gate)} = 10\text{ M}\Omega \parallel 333\text{ M}\Omega = \mathbf{9.7\text{ M}\Omega}$$

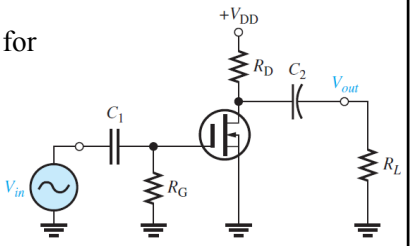
→ $R_{in} \approx R_G$



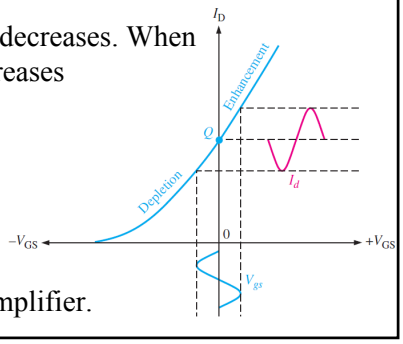
9-1: The Common Source Amplifier

D-MOSFET Amplifier Operation:

- A zero-biased common-source amplifier for *n*-channel D-MOSFET is shown.



- $V_{GS} = 0$ → The signal voltage causes V_{gs} to swing above and below its zero value, producing a swing in I_d above and below Q-point, as shown on characteristic transfer curve



When $V_{gs} < 0$ → the depletion mode, and I_d decreases. When $V_{gs} > 0$ → the enhancement mode, and I_d increases

At $V_{GS} = 0$ → $I_D = I_{DSS}$

→ $V_D = V_{DS}$ can be calculated

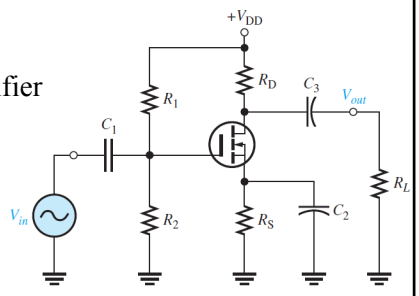
$$V_D = V_{DD} - I_D R_D$$

The ac analysis is the same as for the JFET amplifier.

9-1: The Common Source Amplifier

E-MOSFET Amplifier Operation:

- A voltage divider common-source amplifier for *n*-channel E-MOSFET is shown.
- The gate is biased with a positive voltage such that $V_{GS} > V_{GS(th)}$



- Dc analysis

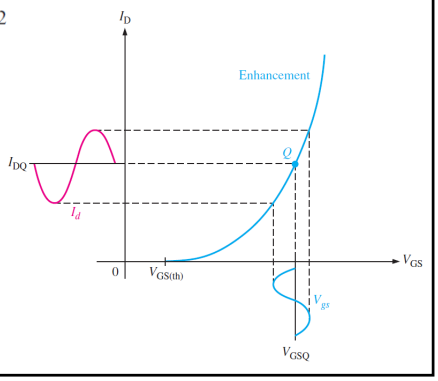
$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

- Ac analysis $R_{in} = R_1 \| R_2 \| R_{IN(gate)}$

where $R_{IN(gate)} = V_{GS}/I_{GSS}$



- Voltage gain is same as for JFET

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{ds}}{V_{gs}} = g_m R_d$$

9-1: The Common Source Amplifier

E-MOSFET Amplifier Operation: Example

A common-source amplifier using an E-MOSFET is shown in Figure 9–17. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. Assume that for this particular device, $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V, $V_{GS(th)} = 2$ V, and $g_m = 23$ mS. $V_{in} = 25$ mV.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{820\,\text{k}\Omega}{5.52\,\text{M}\Omega}\right)15\text{ V} = \mathbf{2.23\text{ V}}$$

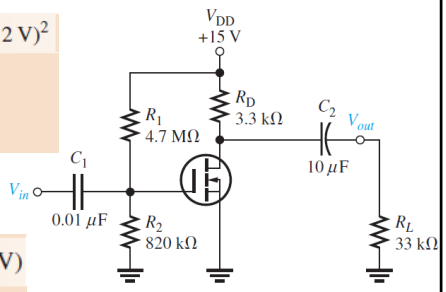
For $V_{GS} = 4$ V, $K = \dfrac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \dfrac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = 50\text{ mA/V}^2$

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(2.23\text{ V} - 2\text{ V})^2 = \mathbf{2.65\text{ mA}}$$

$$V_{DS} = V_{DD} - I_D R_D = 15\text{ V} - (2.65\text{ mA})(3.3\,\text{k}\Omega) = \mathbf{6.26\text{ V}}$$

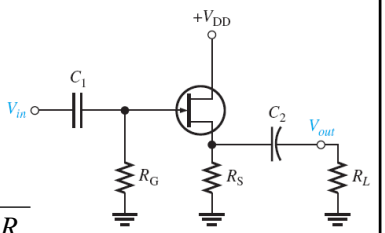
$$R_d = R_D \parallel R_L = 3.3\,\text{k}\Omega \parallel 33\,\text{k}\Omega = 3\,\text{k}\Omega$$

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (23\text{ mS})(3\,\text{k}\Omega)(25\text{ mV}) = \mathbf{1.73\text{ V}}$$



9-2: The Common Drain Amplifier (CD Amplifier) or source follower

- In a CD amplifier, the input signal is applied to the gate and the output signal is taken from the source. There is no drain resistor, because it is *common* to the input and output signals.
- The voltage gain is



$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_s}{V_{gs} + V_s} = \frac{I_d R_s}{V_{gs} + I_d R_s} = \frac{g_m V_{gs} R_s}{V_{gs} + g_m V_{gs} R_s}$$

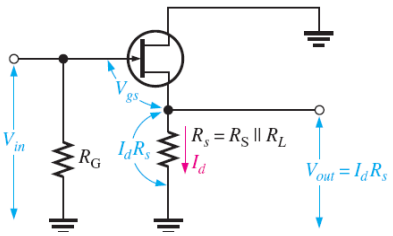
$$\longrightarrow \quad A_v = \frac{g_m R_s}{1 + g_m R_s}$$

If $g_m R_s \gg 1 \longrightarrow A_v \cong 1$

Input Resistance

$$R_{in} = R_G \parallel R_{IN(gate)}$$

where $R_{IN(gate)} = V_{GS}/I_{GSS}$



Ac equivalent circuit

9-2: The Common Drain Amplifier

Example

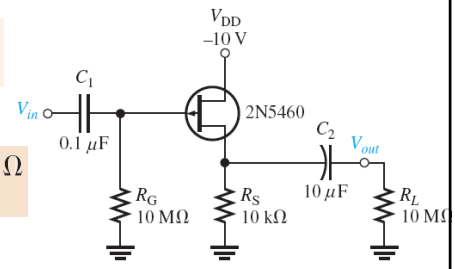
Determine the voltage gain and the input resistance of the amplifier in Figure 9–20. V_{DD} is negative because it is a *p*-channel device. From data sheet $g_m = y_{fs} = 1000\mu S$, $I_{GSS} = 5$ nA (maximum) at $V_{GS} = 20$ V.

Since $R_L \gg R_S$, $R_s \cong R_S$

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(1000\,\mu S)(10\,k\Omega)}{1 + (1000\,\mu S)(10\,k\Omega)} = \mathbf{0.909}$$

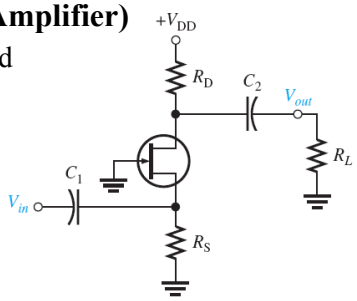
$$R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{20\text{ V}}{5\text{ nA}} = 4000\,M\Omega$$

$$R_{in} = R_G \| R_{IN(gate)} = 10\,M\Omega \| 4000\,M\Omega \cong \mathbf{10\,M\Omega}$$



9-3: The Common Gate Amplifier (CG Amplifier)

- In a CG amplifier, the input signal is applied to the source and the output signal is taken from the drain.
- The voltage gain is



$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_d}{V_{gs}} = \frac{I_d R_d}{V_{gs}} = \frac{g_m V_{gs} R_d}{V_{gs}}$$

$$A_v = g_m R_d \quad \text{where } R_d = R_D \| R_L$$

Input Resistance

$$R_{in(source)} = \frac{V_{in}}{I_{in}} = \frac{V_{gs}}{I_s} = \frac{V_{gs}}{I_d} = \frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$$

$$R_{in} = R_{in(source)} \| R_S$$

9-3: The Common Gate Amplifier (CG Amplifier)

Example

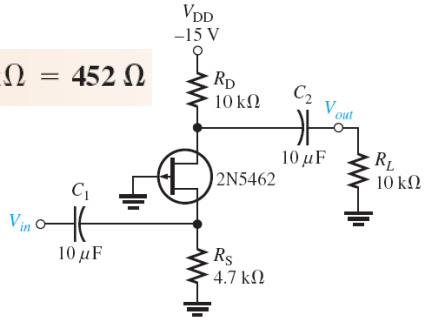
Determine the minimum voltage gain and input resistance of the amplifier in Figure 9–23. V_{DD} is negative because it is a *p*-channel device. $g_m = 2000\ \mu S$ minimum

$$A_v = g_m R_d$$

$$A_v = g_m(R_D \parallel R_L) = (2000\ \mu S)(10\ k\Omega \parallel 10\ k\Omega) = \mathbf{10}$$

$$R_{in(source)} = \frac{1}{g_m} = \frac{1}{2000\ \mu S} = 500\ \Omega$$

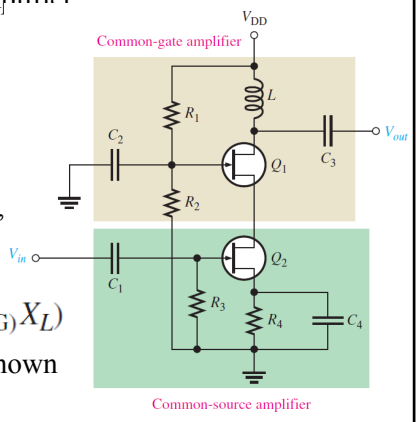
$$R_{in} = R_{in(source)} \parallel R_S = 500\ \Omega \parallel 4.7\ k\Omega = \mathbf{452\ \Omega}$$



9-3: The Common Gate Amplifier (CG Amplifier)

The Cascode Amplifier

- A **cascode** amplifier is one in which a common-source amplifier and a common-gate amplifier are connected in a series arrangement as shown below. As noted from figure, the input resistance ($1/g_m$) for CG amplifier represent the drain resistance R_d for CS amplifier



- The cascode amplifier using JFETs provides a very high input resistance and significantly reduces capacitive effects to allow for operation at much higher frequencies, used for RF (radio frequency), than a common-source amplifier alone

The voltage gain

$$A_v = A_{v(CS)} A_{v(CG)} = (g_{m(CS)} R_d)(g_{m(CG)} X_L)$$

Where X_L is the reactance of the inductor L shown

$$A_v = \left(g_{m(CS)}\left(\frac{1}{g_{m(CG)}}\right)\right)(g_{m(CG)} X_L) \cong g_{m(CG)} X_L$$

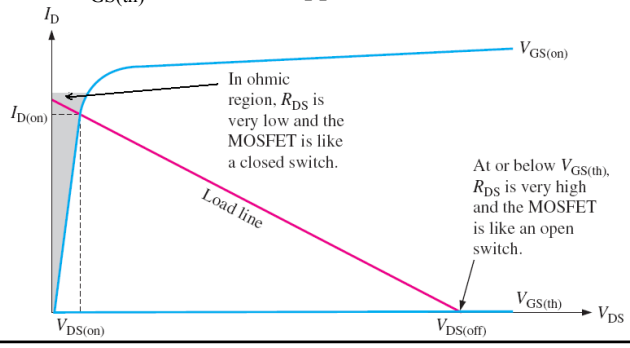
with $g_{m(CS)} \approx g_{m(CG)}$

9-5: MOSFET Analogue Switching

MOSFETs are widely used in analog and digital switching applications. Generally, they exhibit very low *on*-resistance, very high *off*-resistance, and fast switching times.

MOSFET Switching Operation

- E-MOSFETs are generally used for switching applications:
  - When $V_{GS} < V_{GS(th)}$ → MOSFET is *off* → very high R_{DS}
  - When $V_{GS} > V_{GS(th)}$ → MOSFET is *on* → very low R_{DS} (V_{GS} must be sufficiently higher than $V_{GS(th)}$ to be in the upper end of load line in the Ohmic region)



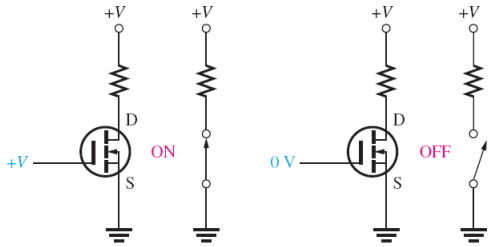
9-5: MOSFET Analogue Switching

MOSFET Switching Operation

- n-channel E-MOSFET operation as a switch

V_{GS} is $+V$ → switch on

V_{GS} is 0 → switch off

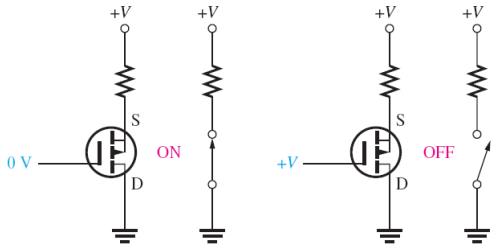


(a) *n*-channel MOSFET and switch equivalent

- p-channel E-MOSFET operation as a switch

V_{GS} is 0 → switch on

V_{GS} is $+V$ → switch off

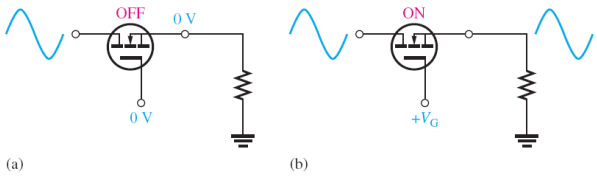


(b) *p*-channel MOSFET and switch equivalent

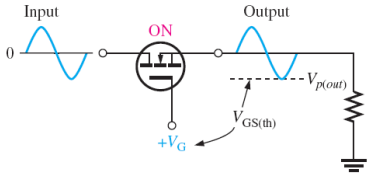
9-5: MOSFET Analogue Switching

The analogue switch

- A basic *n*-channel MOSFET **analog switch** is shown in the figure. The signal at the drain is connected to the source when the MOSFET is turned on by a positive V_{GS} and is disconnected when V_{GS} is 0, as indicated.



- Variable voltage at the source cause variation in V_{GS} → V_{GS} must be ≥ $V_{GS(th)}$ to keep MOSFET maintain conduction (on). Minimum V_{GS} voltage occurs at –ve peak voltage of the output ($V_{p(out)}$)→



$$V_{GS} = V_G - V_{p(out)} \geq V_{GS(th)}$$

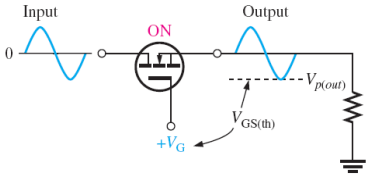
9-5: MOSFET Analogue Switching

The analogue switch: Example

A certain analog switch similar to the one shown in Figure 9–35 uses an *n*-channel MOSFET with $V_{GS(th)} = 2$ V. A voltage of +5 V is applied at the gate to turn the switch *on*. Determine the maximum peak-to-peak input signal that can be applied, assuming no voltage drop across the switch.

The difference between the gate voltage and the negative peak of the signal voltage must equal or exceed the threshold voltage. For maximum $V_{p(out)}$,

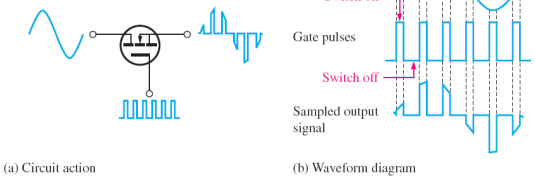
$$V_G - V_{p(out)} = V_{GS(th)}$$
$$V_{p(out)} = V_G - V_{GS(th)} = 5\text{ V} - 2\text{ V} = 3\text{ V}$$
$$V_{pp(in)} = 2V_{p(out)} = 2(3\text{ V}) = \mathbf{6\text{ V}}$$



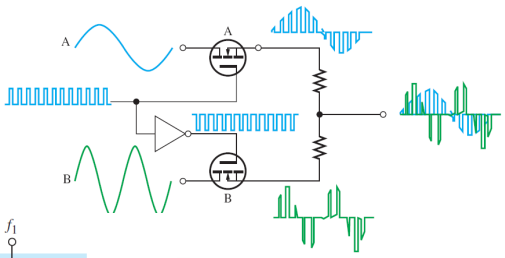
9-5: MOSFET Analogue Switching

The analogue switch: some applications

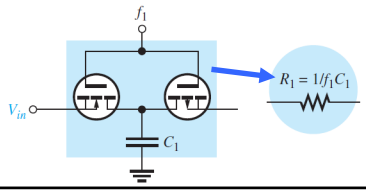
- Sampling circuit: analogue to digital conversion



- Analogue multiplexer: two or more signals are to be routed to the same output



- Switched-Capacitor Circuit: where switch MOSFETs with a capacitor can be used to replace a resistor

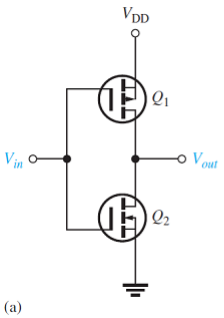


9-5: MOSFET Digital Switching

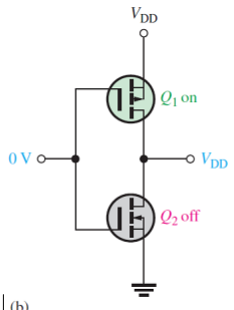
MOSFETs are also used in switching applications in digital integrated circuits

CMOS (Complementary MOS)

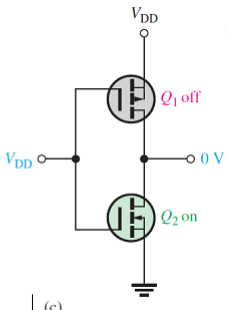
CMOS combines *n*-channel and/or *p*-channel E-MOSFETs in a series arrangement. The shown figure represent a logic ***Inverter Gate***



a) V_{in} can be 0 or 1 ($+V_{DD}$) → V_{out} is the inverse



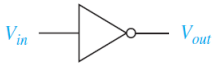
b) $V_{in} = 0$ → Q_1 on and Q_2 off → $V_{out} = +V_{DD}$



c) $V_{in} = +V_{DD}$ → Q_1 off and Q_2 on → $V_{out} = 0$

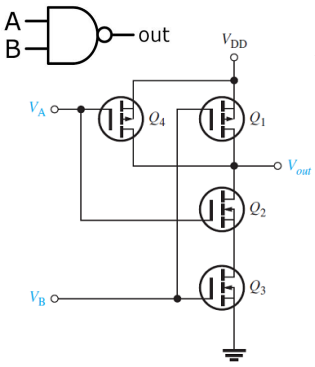
CMOS inverter operation

V_{in}	V_{out}
0	1
1	0



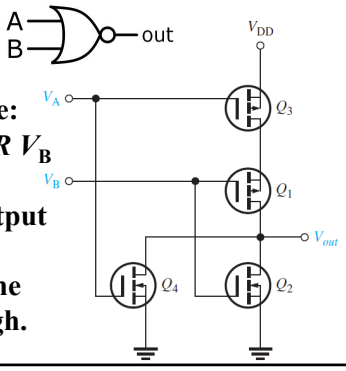
9-5: MOSFET Digital Switching

CMOS (Complementary MOS): *NAND* Gate and *NOR* Gate



■ **NAND Gate: When V_A *AND* V_B are high, the output is low; otherwise, the output is high.**

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	off	on	V_{DD}
0	V_{DD}	off	off	off	on	V_{DD}
V_{DD}	0	on	off	off	off	V_{DD}
V_{DD}	V_{DD}	off	on	on	off	0



■ **NOR Gate: When V_A *OR* V_B *OR* both are high, the output is low; otherwise, the output is high.**

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	on	off	V_{DD}
0	V_{DD}	off	on	on	off	0
V_{DD}	0	on	off	on	off	0
V_{DD}	V_{DD}	off	on	off	on	0